REMARKS

Applicants have amended their claims in order to further clarify the definition of various aspects of the present invention. Specifically, Applicants are adding new claims 27 and 28 to the application. Claims 27 and 28, each dependent on claim 14, respectively recites that the plural semiconductor-mounting substrate portions are side-by-side; and recites that the plural semiconductor-mounting substrate portions are in a plane. Note, for example, Fig. 11f of Applicants' original disclosure.

Applicants respectfully traverse the rejection of their claims as set forth in the Office Action mailed December 29, 2005, and respectfully submit that all of the present claims patentably distinguish over the teachings of the applied reference, that is, the teachings of U.S. Patent No. 5,579,207 to Hayden, et al., under the provisions of 35 USC 102 and 35 USC 103.

It is respectfully submitted that this reference as applied by the Examiner would have neither taught nor would have suggested a substrate for mounting a semiconductor device, as in the present claims, including, inter alia, wherein the substrate has plural semiconductor-mounting substrate portions, each for mounting a respective semiconductor device, with a connecting portion for connecting the plural semiconductor-mounting substrate portions, and a registration mark portion, and wherein each of the semiconductor-mounting substrate portions includes wirings that include an external connection terminal and a specified wire bonding terminal positioned specifically relative to each other, with the connecting portion including an electrically conductive layer. See claim 14.

Furthermore, it is respectfully submitted that the applied reference would have neither taught nor would have suggested such a substrate as in the present claims, having features as discussed previously in connection with claim 14, and,

additionally, wherein the plural semiconductor-mounting substrate portions are side-by-side (see claim 26); or wherein the plural semiconductor-mounting substrate portions are in a plane (see claim 27).

Additionally, it is respectfully submitted that the teachings of the applied reference would have neither disclosed nor would have suggested such a substrate as in the present claims, having features as discussed previously in connection with claim 14, and, additionally, wherein the electrically conductive layer and the wirings are made of a same material (see claim 15); and/or wherein nickel and gold are plated on a surface of the wirings (see claims 16 and 17); and/or wherein the wire bonding terminal is a terminal for connecting a wire from the semiconductor device thereto (see claim 24); and/or wherein the external connection terminal is for electrically connecting the substrate to an outer wiring (see claims 25 and 26).

As is clear from Applicants' disclosure, through use of the substrate as recited in the present claims, including wherein the connecting portion includes an electrically conductive layer, a sufficiently rigid substrate for mounting a plurality of semiconductor devices thereon (which, for example, can later be separated into individual packaged devices), is achieved. In addition, through use of the wirings including the external connection terminal and wire bonding terminal positioned as in the present claims, a relatively small device can be achieved, as compared with, e.g., a device having leads extending outwards of the semiconductor device. Furthermore, through the use of the registration mark portion, the substrate can easily and effectively be positioned for, e.g., mounting and subsequently separating packaged semiconductor devices.

In particular, according to the present invention, wherein the wire bonding terminal is a terminal for connecting a wire from the semiconductor device to such

wire bonding terminal, and especially wherein the external connection terminal is for electrically connecting the substrate to an outer wiring, with the external connection terminal and wiring bonding terminal provided as set forth the present claims, a very compact device which can achieved, for example, a chip scale package can be obtained.

Hayden, et al. discloses a 3-dimensional package of stacked integrated circuit chips, the plurality of stacked chip layers being provided wherein each chip layer includes a substrate or chip carrier having a number of electrically conductive vias extending between its top and bottom sides, with via connecting pads formed on the top and bottom sides of each via. A pattern of electrically conductive traces is formed on one side of the substrate, at least some of which are connected to some of the via pads; and an integrated circuit chip is mounted on the other side of the substrate with its connecting pads wire bonded to some of the electrically conductive traces. This patent discloses that the chip layers are arranged in a stack with the vias of each layer aligned with the vias of an adjacent layer and with the via pads on top and bottom sides of each layer being electrically and mechanically connected to via pads on bottom and top sides, respectively, of adjacent layers. See the paragraphs bridging columns 1 and 2 of this patent. Note also column 4, lines 44-46, together with Fig. 2.

Hayden, et al. goes on to disclose that, as seen in the carrier bottom view of Fig. 2, the carrier includes three registration openings 100, 102 and 104 at three different corners of the carrier. Note column 4, lines 55-63. See also column 6, lines 12-21, disclosing arrangement of the stack on a PC board or other mounting substrate for making physical and electrical connection of the stack to the mounting substrate.

Initially, it is to be emphasized that Hayden, et al. discloses a stack of semiconductor chips, with each chip including a substrate. It is respectfully submitted that this patent would have neither disclosed nor would have suggested the presently claimed invention, including a substrate for mounting semiconductor devices, this substrate having plural semiconductor-mounting substrate portions each for mounting a respective semiconductor device, and with a connecting portion comprising an electrically conductive layer for connecting the semiconductor-mounting substrate portions. From the terms in Hayden, et al. itself, each chip layer includes a substrate, with the substrates being stacked on each other; and it is respectfully submitted that this would have taught away from the substrate having the plural semiconductor-mounting substrate portions, as in claim 14; and, more particularly, the arrangement of such portions as in claims 27 and 28.

In the Examiner's analysis in comparing the teachings of Hayden, et al. to the subject matter of the present claims, the Examiner contends that Hayden, et al. teaches "a" substrate. Such interpretation by the Examiner is respectfully traversed, particularly in view of the express disclosure in Hayden, et al. that each chip layer includes a substrate, the stacked structure including multiple chip layers and therefore multiple substrates.

Applicants note the statement by the Examiner in the first paragraph of page 2 of the Office Action mailed December 29, 2005. As can be seen in the foregoing, it is respectfully submitted that the presently claimed subject matter would have neither been disclosed nor would have been suggested by the teachings or suggestions from Hayden, et al. In any event, Applicants respectfully reserve the right to submit a translation of appropriate priority application(s) under 37 CFR 1.55.

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In view of the foregoing comments and amendments, reconsideration and allowance of all claims presently in the application are respectfully requested.

Applicants request any shortage in fees due in connection with the filing of this paper be charged to the Deposit Account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (case 648.43481VC5), and credit any excess payment of fees to such Deposit Account.

Respectfully submitted,

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